WHAT IS CLAIMED IS:

1. A duplex device, comprising:

an active module having a primary central processing unit that carries out control and data processes, a primary arbiter that arbitrates the use of a primary bus, a primary memory controller that controls access to a primary memory, a primary D-channel controller that provides a primary first-in first-out (FIFO) memory for the communication of parallel data on a duplexing path, and a primary C-channel controller that communicates primary status information of the active module;

a standby module having a secondary central processing unit that carries out control and data processes, a secondary arbiter that arbitrates the use of a secondary bus, a secondary memory controller that controls access to a secondary memory, a secondary D-channel controller that provides a second FIFO memory for the communication of the parallel data on the duplexing path, and a secondary C-channel controller that communicates secondary status information of the standby module;

a C-channel that exchanges the primary and secondary status information between the primary and secondary C-channel controllers to support duplexing logic between the active module and the standby module; and

a D-channel that supports access to the primary and secondary memories by both the primary and secondary central processing units.

2. The duplex device of claim 1, wherein each of the primary and secondary C-channel controllers identifies the primary status information and the secondary status information, based on the values of a self-side active signal, a self-side normal signal, a pair-side active signal, and a pair-side normal signal, and determines which one of the active and standby modules is operating in an active mode and which is operating in a standby mode.

3. The duplex device of claim 2, wherein:

the self-side active signal transmitted by the primary C-channel controller is designated as the pair-side active signal, when received by the secondary C-channel controller;

the self-side normal signal transmitted by the primary C-channel controller is designated as the pair-side normal signal, when received by the secondary C-channel controller;

the self-side active signal transmitted by the secondary C-channel controller is designated as the pair-side active signal, when received by the primary C-channel controller; and

the self-side normal signal transmitted by the secondary C-channel controller is designated as the pair-side normal signal, when received by the primary C-channel controller.

4. The duplex device of claim 2, wherein each of the primary and secondary D-channel controllers obtains the primary status information and secondary status information, from the primary or secondary C-channel controller of its respective one of the active or standby modules and executes a duplexing operation, as a master or a slave of a Power Personal

Computer (PPC) bus, in a communication direction of the D-channel determined by a comparison of the primary status information and the secondary status information.

5. A method of operating a duplex device, comprising:

(a) reading a secondary status of a secondary module, via a C-channel, with a primary module, comparing the secondary status with a primary status of the primary module to obtain a first result, determining a direction of a D-channel based upon the value of the first result, and determining which one of the primary and secondary modules is an active module based upon the value of the first result;

(b) reading only the contents of a first memory in the active module to a processor within the active module that requested the contents, when the processor performs a memory read operation of the first memory, and concurrently writing data to the first memory and to a second memory in the one of the primary and secondary modules that is not the active module and is, therefore, designated a standby module, when the processor performs a memory write operation; and

(c) recognizing, with the standby module, that a fault has occurred in the active module by identifying an abnormal signal communicated by a C-channel controller of the active module, changing the active module to a standby mode of operation;

(d) changing the standby module to an active mode of operation;

(e) changing the primary module or the secondary module that has the active mode of operation to be the active module; and

(f) changing the primary module or the secondary module that has the standby mode of operation to be the standby module.

6. The method of claim 5, wherein the active module executes the memory write operation to the second memory, via the D-channel, and each of a primary D-channel controller and a secondary D-channel contoller executes a duplexing operation, while serving as a master or slave in a power PC (PPC) bus.

7. The method of claim 5, wherein step (b) further comprises:

analyzing a transfer type signal and an address in a first D-channel controller of the active module to obtain a second result;

if the second result is determined to be the memory read operation addressed to the first memory, reading the addressed contents only from the first memory and if the second result is determined to be either the memory write operation or the memory read operation addressed to the second memory, writing the address, the transfer type signal, and a transfer size signal from a first FIFO memory of the first D-channel controller to a second FIFO memory of a second D-channel controller of the standby module;

when an empty flag signal is asserted from the second FIFO memory, sending a bus request signal from the second D-channel controller to a bus arbiter of the standby module and receiving a bus grant signal at the second D-channel controller from the bus arbiter;

after the bus grant signal is received, generating a transfer start signal from the second D-channel controller to a second memory controller of the standby module and transmitting the address to the second memory via an internal bus operation of the standby module; and

if an operation completion signal is generated from the second memory controller, returning the bus grant signal to the bus arbiter.

8. The method of claim 7, wherein the first FIFO memory writes the address, the transfer type signal and the transfer size signal to the second FIFO memory during the memory read operation.

9. The method of claim 7, wherein the address determines whether the contents are read from the first memory or the second memory.

10. The method of claim 9, wherein an address region is divided into two regions, wherein a first region of the two regions comprises memory addresses common to both the first memory and the second memory and a second region of the two regions comprises memory addresses used only for reading from the second memory.

11. The method of claim 10, wherein the first D-channel controller recognizes both the memory read operation having the second region address and the transfer type signal and

converts the second region address into a corresponding first region address and writes the corresponding first region address to the second FIFO memory.

12. The method of claim 7, wherein the first FIFO memory, at the time of the memory write operation, writes the address, the transfer type signal and the transfer size signal to the second FIFO memory and the second D-channel controller transmits the address via an internal bus of the standby module.

13. The method of claim 7, wherein if the memory read operation or the memory write operation is completed abnormally, the second D-channel controller inputs a transfer error acknowledge signal and asserts a D-channel error signal to the first D-channel controller, thereby generating a D-channel interrupt signal to the active module.

14. The method of claim 7, wherein if the memory read operation from the second memory is completed normally, the first D-channel controller communicates a primary transfer completion message to a first memory controller of the active module and the second D-channel controller communicates a secondary transfer completion message to the second memory controller.

15. The method of claim 7, wherein if the memory write operation to the second memory is completed normally, the second D-channel controller informs the first D-channel controller of a write completion.

16. The method of claim 5, wherein step (c) further comprises:

generating an interrupt in the active module, if the fault occurs;

if the interrupt is generated in the active module, writing register information of a first D-channel controller, during a delay time, to a second FIFO memory of a second D-channel controller in a burst mode;

if the write operation in the burst mode is completed, asserting a self-side abnormal status and a first self-side active status of the C-channel controller of the active module to a high state and transmitting an assert signal to the second D-channel controller; and

asserting a second self-side active signal of the standby module to a low state; and

changing the standby module to the active mode of operation.

17. A duplex device, comprising:

a first device and a second device of the duplex device each having a D-channel controller and a C-channel controller;

a D-channel interconnecting the D-channel controllers of the first and second devices to convey at least one of data signals, address signals, and control signals; and

a C-channel interconnecting the C-channel controllers of the first and second devices to convey status signals, wherein

the C-channel controller of the first and second devices each monitor a subset of the C-channel status signals to determine which of the first and second devices has an active mode status and which has a standby mode status, and

both the active mode status and the standby mode status are identified by a self-side normal signal and a pair-side active signal.

18. The duplex device of claim 17, wherein:

the active mode status is identified by a true state existing on the self-side normal signal and a false state existing on the pair-side active signal, and

the standby mode status is identified by other combinations of the true and false states existing on the self-side normal and pair-side active signals.

19. The duplex device of claim 18, wherein:

whichever one of the first and second devices that has the active mode status, generates the address signals conveyed by the D-channel.

20. The duplex device of claim 18, wherein each of the first and second devices share a common address bus and a common data bus and further comprises:

a communication processor that communicates input and output (I/O) information between the duplex device and external devices;

a central processing unit that controls communication processes within the respective first and second devices;

a memory that stores retained information;

an arbiter that arbitrates the use of the common data bus, wherein

one of the first and second devices has the active mode status to generate the address signals conveyed by the D-channel and to control a read access and a write access to each memory of the first and second devices.

21. The duplex device of claim 20, wherein:

within both of the first and second devices, respectively, the communication processor, the central processing unit, the memory, and the D-channel controller share the common data bus and the common address bus.

22. A method of implementing a duplex device that has a first device and a second device, comprising:

reading a first status of the first device and a second status of the second device;

setting one of the first and second devices to an active mode status and the other of the respective devices to a standby mode status based on the first and second status, wherein

both the first status and the second status are identified by a self-side normal signal and a pair-side active signal.

23. The method of claim 22, wherein:

the active mode status is identified by a true state existing on the self-side normal signal and a false state existing on the pair-side active signal, and

the standby mode status is identified by other combinations of the true and false states existing on the self-side normal and pair-side active signals.

24. The method of claim 22, wherein:

the first and second devices each have a communication processing unit, a central processor, a memory, and a D-channel controller, which share both a common address bus and a common data bus;

the first and second devices each have a C-channel controller that communicates with the central processor of the respective first and second devices;

a D-channel interconnects the D-channel controllers of the first and second devices to convey data signals, address signals, and control signals; and

a C-channel interconnects the C-channel controllers of the first and second devices to convey the first and second status between the first and second C-channel controllers, wherein

one of the first and second devices has the active mode status to generate the address signals conveyed by the D-channel and to control a read access and a write access to the memories of both the first and second devices.